Clock Recovery Instrument

BERTScope® CR Series Data Sheet

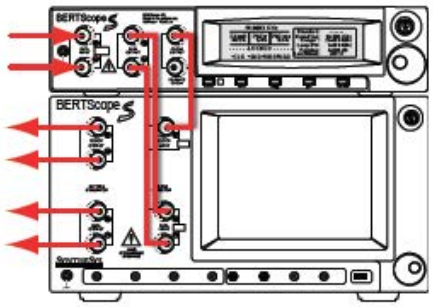
Features & Benefits

- Instrumentation Quality Clock Recovery
- 150 Mb/s to 28.6 Gb/s with Continuous Data Rate Coverage to include Next-generation I/Os including PCIe 3.0, 10GBASE-KR, 16xFC, 25/28 G CEI, and 100GBASE-LR-4/100GBASE-ER-4
- Accurate, Variable Loop Bandwidth from 100 kHz to 12 MHz, with Optional 24 MHz for the Jitter Transfer Function (JTF) Bandwidths of USB 3.0, SATA 6G, and PCIe Gen3
- Accurate, Adjustable, Self-measured, and Displayed PLL Loop Bandwidth, Peaking, and JTF – Get the "Golden PLL" Response Needed for Standards Compliance Testing
- Programmable Peaking Adjustment with First- and Second-order Rolloff Capability
- USB Control Interface Integrated into BERTScope View, or Stand-alone with included BERTScope PC Software
- DC-coupled Data Through Path for Accurate Signal Integrity
- Full and Divided Clock Outputs with Selectable Divide Ratios. Full-rate Clock Output up to 14.3 Gb/s, Half-rate Clock Output from 14.3 Gb/s to 17.5 and 28.6 Gb/s
- Built-in Equalizer Function enables Clock Recovery under High ISI Input Conditions
- Data Measurement Capability
  - Edge Density Measurement – Determine the mark density of the signal under test
  - Spread Spectrum Clock Waveform View including dF/dt
- Ideal for Spread Spectrum Clock (SSC) Applications with Large Frequency Excursions
- Optional Direct Spectral Analysis of Jitter Components when under USB Control from BERTScope or on PC using Provided “stand-alone” SW.
- Optional “Spectrum Analyzer” Display with Cursor Measurements of Jitter Amplitude and Frequency
- User-settable Frequency-gated Measurements for Band-limited Integrated Jitter Optionally Available
  - Preset Band Limits for PCI Express Gen2 Jitter Spectrum
- Optional PCIe 2.5 and 5 Gb/s PLL Loop Analysis (Also requires jitter analysis option)
- CR175A and CR286A offer Optional Higher-sensitivity Data Inputs with Clock Recovery on Signals as Small as 40 mV Amplitude (Single ended), 20 mV Amplitude (Differential) – No DC-coupled Data Through Path with this Option

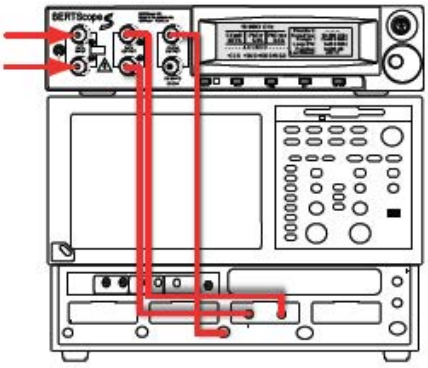
Applications

- Design/Verification of High-speed I/O Components and Systems
- Signal Integrity Analysis
- Certification Testing of Serial Data Streams for Industry Standards

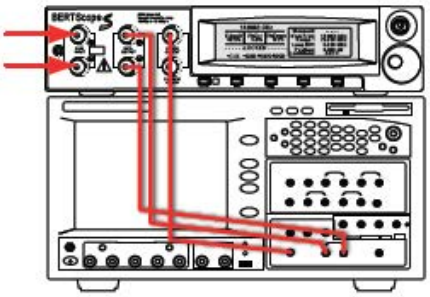
Tektronix®



Connecting the BERTScope CR clock recovery instrument to the BERTScope Analyzer

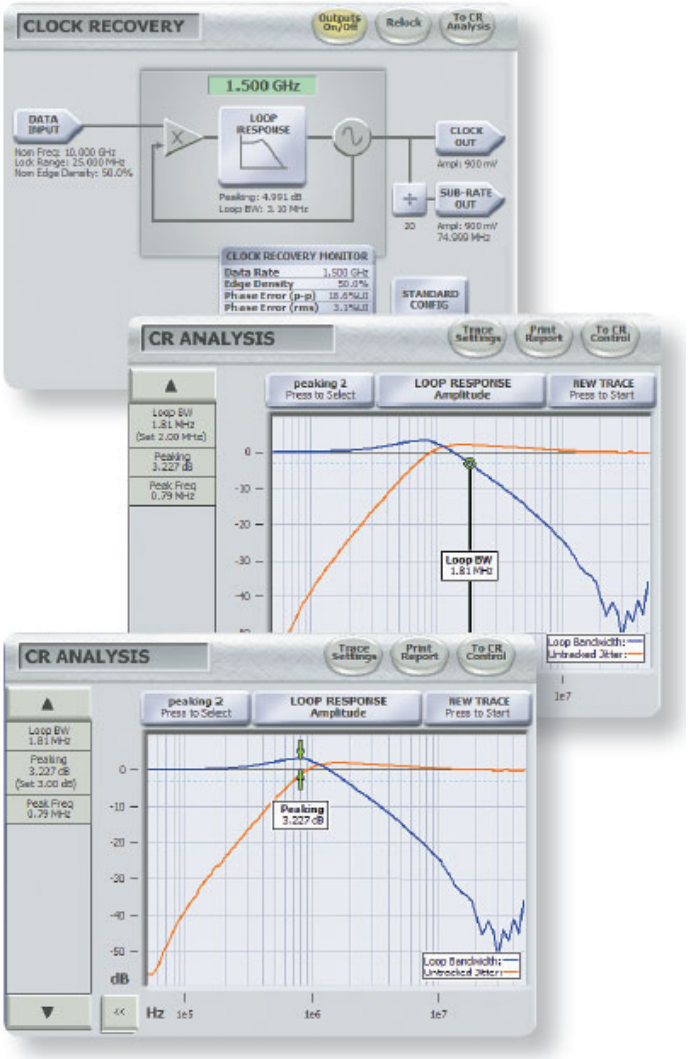


Connecting the BERTScope CR clock recovery instrument to a sampling oscilloscope



Connecting the BERTScope CR clock recovery instrument to a BERT

The BERTScope CR Series can be used with any sampling oscilloscope, BERT, or pattern generator.



The BERTScope CR Series Work Seamlessly with BERTScope Analyzers – You can utilize the clock recovery instrument with the BERTScope Analyzer by connecting the USB cable between the two instruments. The graphing capability can be displayed on the BERTScope Analyzer by pressing the "To CR analysis" soft key.

Compliant Clock Recovery

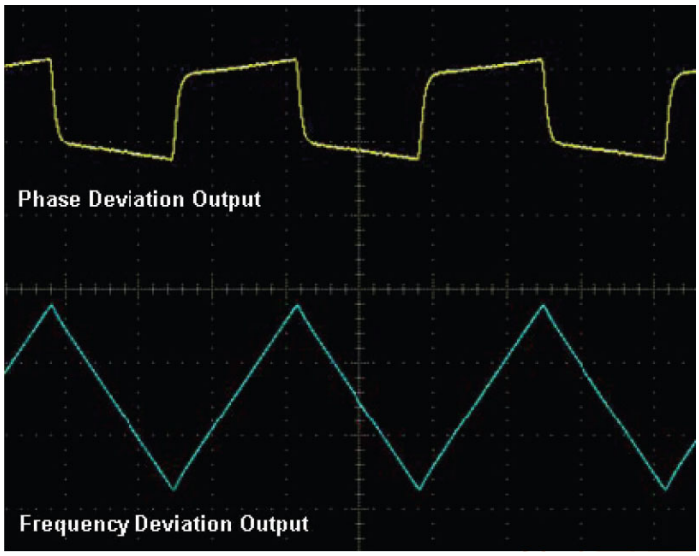
Many communication standards now specify that jitter testing must be carried out using a reference clock that has been derived from the data signal. Typical Phase Lock Loop (PLL) characteristics are specified in terms of the –3 dB bandwidth of the recovery loop, the rate of rolloff of the frequency response, and the degree of response peaking allowable.

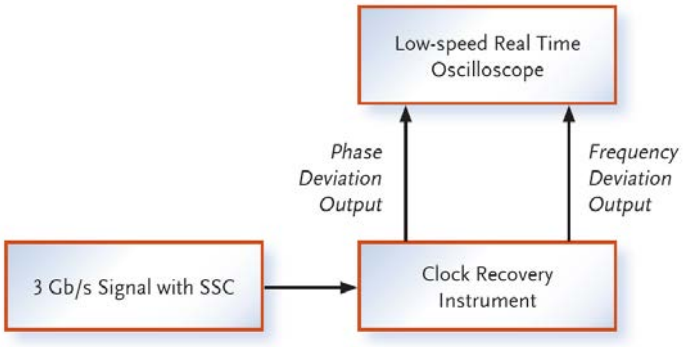
The BERTScope CR Series advanced architecture measures and displays the PLL frequency response from 100 kHz to 12 MHz; the highest loop bandwidth available for jitter testing on the market today. The first clock recovery instruments to allow full control of parameters including loop bandwidth, peaking/damping, and rolloff.

Design and test engineers can now find and lock onto signals of undefined or unknown data rate. The engineer can recover full-rate clocks, including spread spectrum clocks, for signals at data rates from 150 Mb/s to 12.5 Gb/s, and 14.2 Gb/s with extended data rate option. The engineer has full control of key parameters for variable loop bandwidth, peaking/damping and first- and second-order rolloffs, optimizing jitter tracking.

Golden PLL

Many test standards require the use of a Golden PLL (Phase Lock Loop). Control of the BERTScope CR Series variable loop bandwidth allows for control of the jitter transferred to the recovered clock. When the loop bandwidth setting is narrow, much of the high-frequency jitter is removed from the clock signal. The narrowest LBW setting is desirable when a clock with the lowest possible jitter is required. When the loop bandwidth setting is wide, jitter is transferred to the recovered clock, emulating a clock signal similar to the CDR of the receiver under test. Each standard provides an optimum LBW setting for clock recovery often called the Golden PLL.

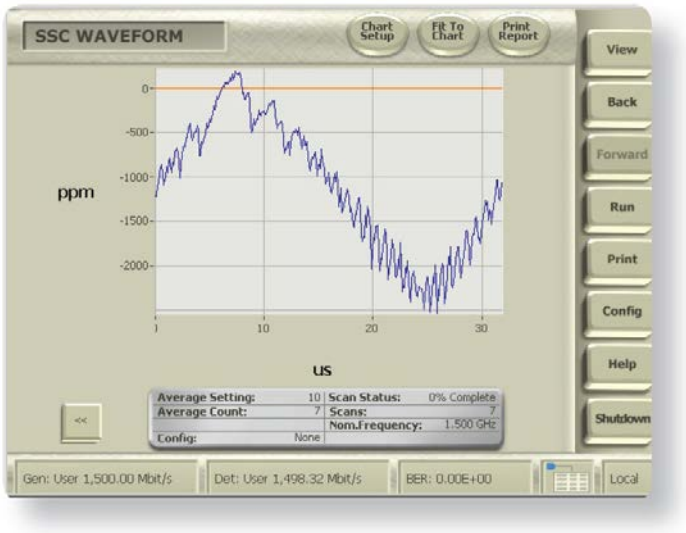




Recover Spread Spectrum Clocks for Testing to Electrical Serial Bus Standards

Spread Spectrum Clocking (SSC) is an increasingly required feature of serial bus standards. When employed, it can prove difficult to track but its effect must be included in test. These instruments are able to track SSC correctly with large frequency excursions up to 5000 ppm, making them unique amongst clock recovery test solutions. The BERTScope CR Series is the first clock recovery instrument to recover clocks from spread spectrum clocked signals used in Serial ATA, SAS, PCI Express, and USB applications.

Spread spectrum clocks exhibit low-frequency (30-33 kHz) modulation, for example, resulting in 225 UI (Unit Interval) deviation when imposed on a 3 Gb/s data signal. This frequency deviation is tracked accurately by the clock recovery instrument when the optional 5-piece cable set is used with the BERTScope CR Series and BERTScope Analyzer. This cable set is matched to compensate for the 5 ns delay in BERTScope Analyzer with SSC signals, thus avoiding jitter amplification.

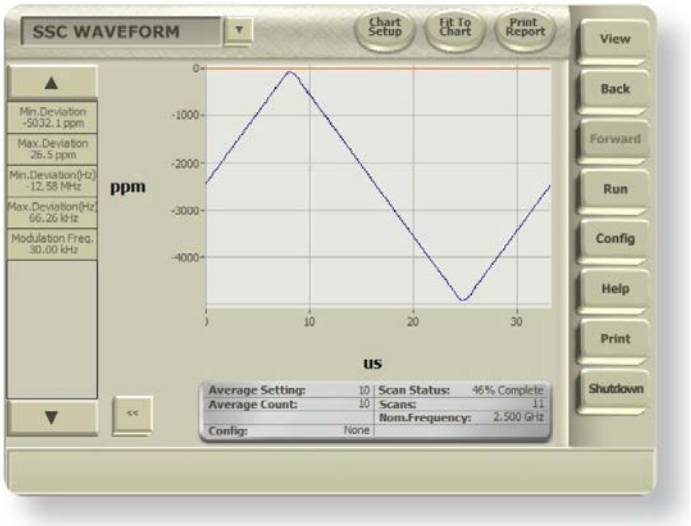


Excessive noise in the SSC modulator may cause tracking problems in the receiver CDR, resulting in bit errors.

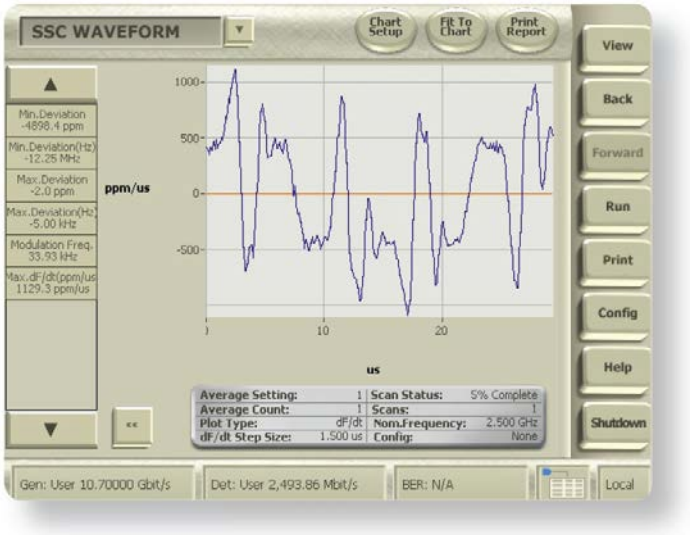
A signal with SSC was measured with the BERTScope CR Series. Outputs on the rear panel of the instrument provide monitoring points to view the loop behavior. When viewed on a low-bandwidth, real-time oscilloscope, the triangular waveform characteristic of SSC is visible in the lower trace. The upper waveform displays the difference in phase between data input and clock recovery output.

View and Measure SSC Modulation

The BERTScope CR Series instruments also allow you to view and measure SSC generated in your system. Problems with the SSC modulation waveform can result in clock rate deviation beyond the capability of the channel or receiver. Excessively fast transitions often cause bit errors, as the receiver CDR cannot track the fast change. Conversely, modulation with long periods of no clock rate change cause energy peaks in parts of the spectrum, resulting in EMI (Electro-Magnetic Interference) which SSC is supposed to reduce.



Cleaner SSC modulation.



A revealing dF/dT waveform showing poor performance.

The SSC Waveform view provides a calibrated plot of the SSC modulation, allowing the user to instantly see if any of these modulation problems exist. The vertical axis represents the carrier deviation, and can be scaled in units of either frequency deviation (PPM) or time (ps).

To avoid the tracking and possible EMI problems from incorrect deviation rates, some of the new serial data standards are specifying the minimum and maximum rate of change of the SSC carrier frequency. The BERTScope CR Series can directly display the dF/dt function, and provide a parametric measurement of the minimum and maximum peaks.

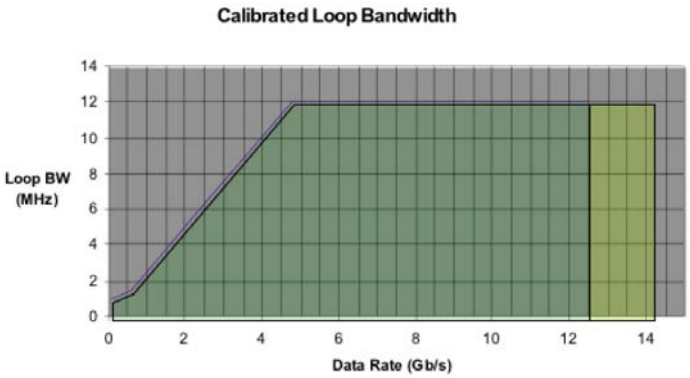
User Interface

The instruments can be used with the BERTScope or in stand-alone operation. Inexperienced users and experts alike will respond to the same ease and accuracy already available in the BERTScope Analyzer. Perfect companions to the BERTScope, the clock recovery instruments smoothly integrate with the analyzer, seamlessly sharing a common user interface. A single USB connection and supplied high-quality microwave coax cables connect the two units together – that is all that is required to start measurements. The BERTScope automatically senses the presence of the clock recovery instrument, and control is achieved through the Clock Recovery setup screen. It's that simple. The same information is also immediately available on the front-panel display, showing parameters such as the PLL bandwidth, lock status, bit rate, peaking, and rolloff. The system is designed to make sure that you are always aware of the test conditions, always aware of the factors in play that will affect your measurement results.

Graphing capability on the BERTScope Analyzer allows users to plot loop response and inverse response curves for the settings in use. The –3 dB point and peaking values are also measured and clearly displayed.

For engineers wanting to utilize test equipment already available on their lab bench, the same control views are available on a PC running BERTScope PC stand-alone software, which is included with the product. Interface to the PC is through a standard USB port. In addition, the instrument can be controlled directly through the front-panel display and knob. In keeping with the BERTScope family's philosophy of being the easiest-to-use signal integrity tools available, the clock recovery instruments provide the information you most need, right up front. For easy verification of compliance, the correct characteristics are automatically set when a given standard is selected from a pull-down menu. However, for users wanting to explore the limits of their designs, full control of parameters is also easily available. A good example of this is for systems where restricting the buildup of jitter is critical. Clock recovery plays a crucial role in this, and the ability to emulate a clock recovery source with excessive peaking is a great way of understanding the system sensitivity to jitter gain. Each instrument has variable jitter peaking that goes way beyond simple compliance, and allows jitter gain in excess of 10 dB if desired.

Remote control of the instrument is easily accessible by USB through the BERTScope Analyzer. TCP/IP and GP-IB protocol interfaces are supported by USB and the software developers kit.



Clock Recovery Loop Bandwidth versus Data Rate – The BERTScope CR Series has a variable loop bandwidth from 100 kHz to 12 MHz. The loop bandwidth is calibrated when operating within the range shown in green in the plot to the left.

Importance of Data and Recovered Clock Path Delay Matching

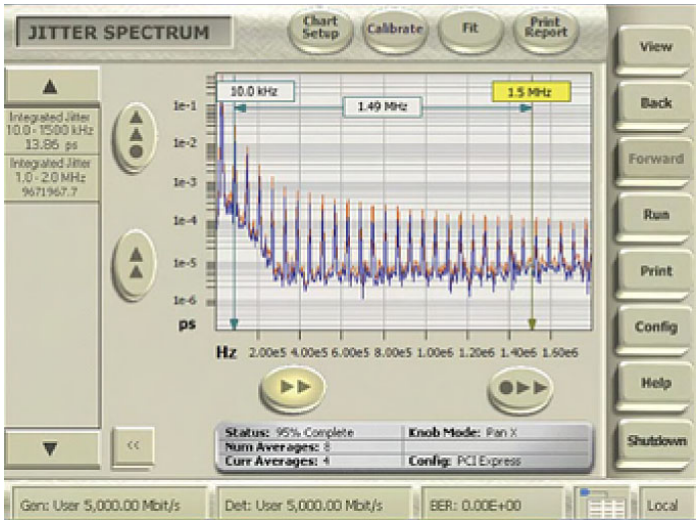
When recovering a clock with SSC modulation or containing a large amount of periodic jitter, it is important to precisely match the delay path of the data signal and recovered clock between the BERTScope CR Series and the test instrument. The data path must have additional delay added corresponding to the trigger latency between the clock edge at the instrument clock or trigger input, and the instant when the instrument actually samples the data. Without matching, at high data rates this delay can be several hundred or even thousand unit intervals. This could have the apparent effect of reduced eye timing margin in masks, higher bit error rates, and inflated jitter measurements.

When the BERTScope CR Series is used with a BERTScope Analyzer, this problem is eliminated by using the precision Matched Cable Set. The set is composed of high-quality low-loss cables, which are carefully matched for differential phase and delay for use with the BERTScope. The set consists of five cables: a pair of phase-matched cables for CR data input, a pair of phase- and delay-matched cables for the data signal between the CR and BERTScope error detector inputs, and a delay-matched cable for connecting the CR clock output to the BERTScope clock input.

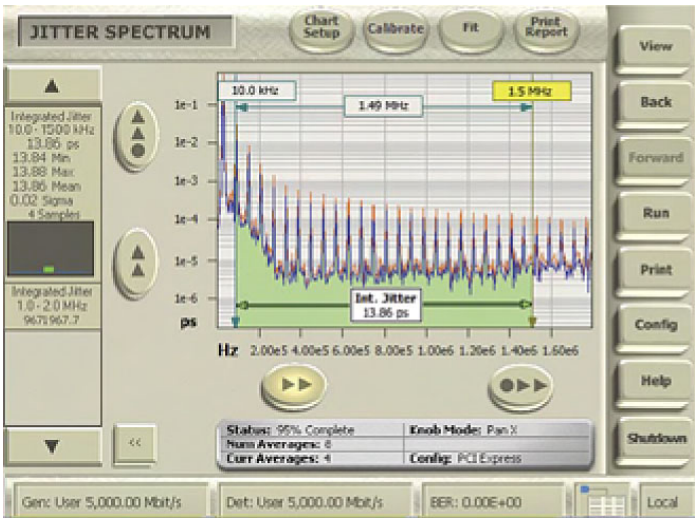
Jitter Spectrum Display

The BERTScope CR Series options 12GJ, 17GJ, and 28GJ feature all of the clock recovery capability and performance of the BERTScope CR Series, with the addition of a powerful jitter measurement and analysis tool – Jitter Spectrum. The Jitter Spectrum view is a plot of jitter magnitude versus frequency. The Jitter Spectrum is a powerful tool for quantifying and isolating the source of jitter components in the device under test. Frequency peaks from unrelated clocks, switching power supplies, and other periodic jitter that is uncorrelated with the data clearly show up in the “spectrum analyzer” type display. The vertical axis is scaled in either % of UI or time. Either linear or log scaling can be selected.

Optional 5-piece Matched Cable Set.



Jitter Spectrum display.



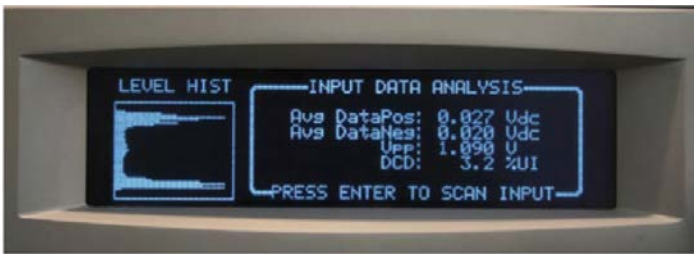
Frequency-gated measurement.

Frequency-gated Measurement

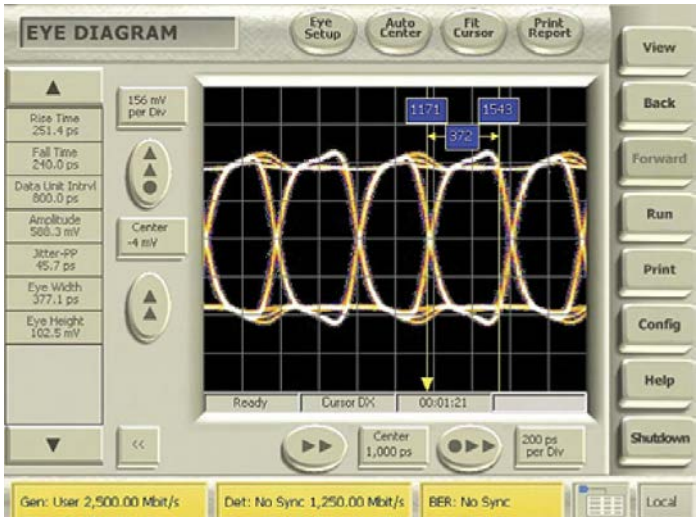
Because the clock recovery process tracks the lower-frequency components in a serial data receiver, the system is generally less sensitive to low-frequency jitter components than to the higher-frequency ones. This varying sensitivity to different frequency components is factored into the compliance tests of various serial data standards, such as second-generation PCI Express. Thus, the ability to measure the magnitude of the jitter components emitted from a transmitter in various frequency bands is important for system validation. The BERTScope CR Series features a band-selected integrated jitter measurement. The user enters the lower and upper limits of the frequency band which the jitter measurement is to be integrated over. A real-time display provides the total integrated jitter within this band. Up to three different simultaneous frequency bands can be entered in the instrument.

Help Isolating Jitter Sources

Periodic jitter components uncorrelated to the data are often caused by coupling of system clocks, crosstalk from uncorrelated data lines, power-supply ripple pattern dependent jitter, etc. These show up as sharp frequency peaks in the jitter display. Cursor measurements allow the user to quickly find the frequency associated with the suspect peak.



DCD data pattern.



DCD jitter measurement.

Duty Cycle Dependent Jitter Measurement

Jitter components can often be related to the data pattern. Duty Cycle Dependent Jitter (DCD) occurs when consecutive bits in the data pattern have unequal lengths. The unequal lengths can be either due to 1s and 0s having different durations or due to the use of sub-rate clocks. For example, a half-rate clock would use a delayed version of its rising edge to clock the second of two consecutive bits. If the delay is different from the nominal unit interval (bit length) then every two bits become a sequence of a long bit followed by a short bit. The BERTScope CR Series can directly measure the DCD in the incoming data stream and report the result in percentage of the unit interval (UI) on the front-panel display.

Powerful Tools to Analyze Jitter

Measurement of the total jitter in a serial data signal provides useful information to predict the accuracy of the system. However, a total jitter number does not provide very much information on the nature of the jitter. This information is necessary to determine the susceptibility of the receiver to various jitter components, and is useful to identify the source. The BERTScope CR Series clock recovery instrument provides powerful jitter analysis capability.

Compliant Clock Recovery for 100 Gb Ethernet and OIF-CEI 28G

The BERTScope CR286A is designed to support emerging high-speed standards such as 100 Gb Ethernet (100 GbE), which operates at a line rate of 25.78125 Gb/s. The CR286A goes a step further with a maximum data rate of 28.6 Gb/s to support OIF-CEI 28G. These instruments have all the core features of the CR125A, the award-winning BERTScope clock recovery product, with extended locking range to 26 and 28.6 Gb/s.

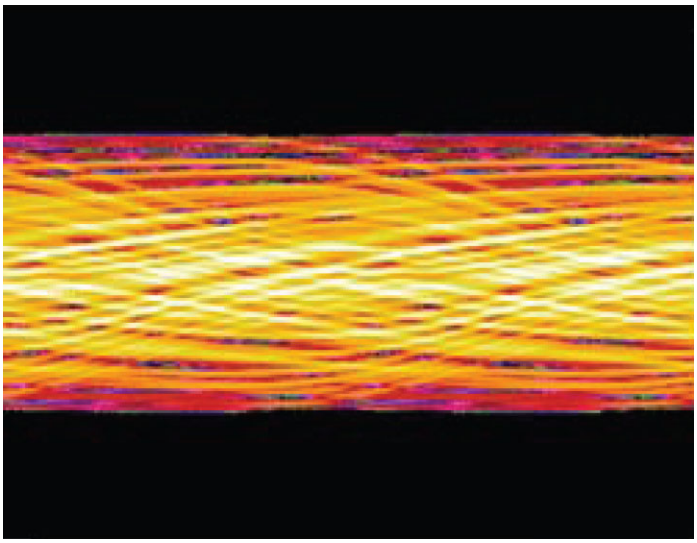
BERTScope CR Series High-sensitivity Model for Low-amplitude Signals

The CR175A and CR286A with Option HS include the same features as the CR models, but with higher input sensitivity for applications involving small signals down to 40 mV (single ended) or 20 mV (differential). This is achieved by removing the power tap-offs from the instrument, allowing the user to access the full sensitivity range. The HS option is ideal for optical applications, where small amplitude signals are common, or for electrical test setups where the extra sensitivity is critical. It offers total control over what fraction of the signal should be dedicated to clock recovery.

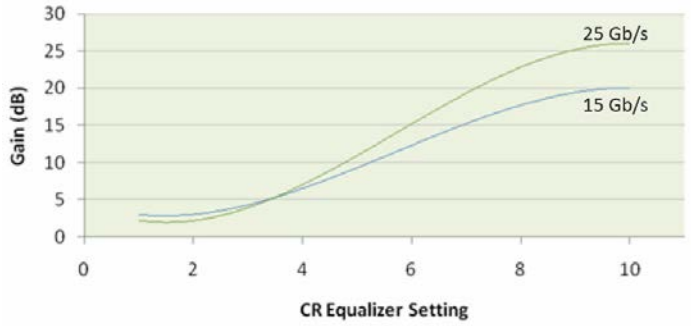
Recover Clocks under Closed Eye Signal Conditions

The BERTScope CR family has built-in equalization, so engineers can recover a clock even when the data input signal suffers ISI from frequency-dependent loss conditions that close the eye completely.

At high bit rates such as the 100 GbE rate of 25.78125 Gb/s, inter-symbol interference that was a problem at 10 Gb/s can pose an even greater threat, turning a partially open eye into one that is completely closed. With built-in linear equalization, you can rely on the BERTScope CR Series to recover a clock while adhering to the loop bandwidth and peaking conditions you have set. This makes triggering a downstream instrument such as a BERTScope or Tektronix oscilloscope easy, while remaining compliant with the “Golden PLL” requirements in the high-speed standard of interest. The data signal through path is unaffected by the clock recovery equalization.



The BERTScope CR Series can recover a clock under harsh conditions such as a 10 Gb/s PRBS-31 data pattern with 71” of trace on the ISI board – a capability that becomes even more important at 25.78 Gb/s.



Gain versus Equalizer Setting – This graph shows approximate equalizer gain in dB versus the equalizer setting in the CR at 15 and 25 Gb/s input data rate. For the highest equalizer setting at 25 Gb/s input data rate, more than 20 dB of linear equalization is applied to the input, enabling clock recovery on signals that would normally not achieve successful lock. The equalizer operates over the full data rate range of the CR.

Characteristics

CR125A/175A/286A

Instrument Specifications

Characteristic	Description
Data Interfaces	50 Ω differential or single-ended, DC coupled. APC 3.5 user-replaceable Planar Crown® adapter
Data Rate Coverage	150 Mb/s to 28.6 Gb/s (12.5 Gb/s for CR125A, 17.5 Gb/s for CR175A)
Data Insertion Loss	2 dB (min), 2.6 dB (typical), 3 dB (max) from data input to data output
Data Input Voltage Range	–5 V (min), +5 V (max)
Input Sensitivity	100 mV single ended (typical) 50 mV differential (typical)
Measured Edge Density Resolution	±1%
Measured Phase Deviation	Displayed as % RMS and % peak-peak, 10-90% peak-peak available range
Clock Outputs	
Clock Interfaces	50 Ω single-ended, AC coupled. APC 3.5 user-replaceable Planar Crown® adapter
Clock Output Range	150 MHz to 12.5 GHz (full-rate clock output)
Loop Bandwidth	100 kHz - 12 MHz variable
Loop Bandwidth Accuracy	±10% (1100 pattern)
Locking Range	50 MHz default, adjustable to 10-500 MHz
Peaking	0-6 dB from 500 kHz - 12 MHz, 0 dB from 100 kHz - 500 kHz
Peaking Accuracy	Greater of ±10% of setting, or 0.5 dB
Frequency Response	–20 dB/decade to –40 dB/decade
Intrinsic Jitter (Typical)	70 fs (typical), 250 fs_{RMS} (max), measured at 800 mV_{p-p} input amplitude, 10 Gb/s, 1010 pattern, 2 MHz loop bandwidth setting, and 0.5 dB peaking
Output Frequency Deviation Tracking Range (Tracking 30-33 kHz Triangle Modulated SSC)	+500/–5500 ppm (+0.05/–0.55%)
Minimum Input Return Loss	15 dB
Output Waveform Rise/Fall Times (20/80%)	25 ps (typical), 30 ps (max)
Output Amplitude	250 mV (min) 900 mV (max) at clock rates ≤12.5 Gb/s 700 mV (max) at clock rates >12.5 Gb/s
Output Amplitude Setting Accuracy	Greater of 10% or 30 mV, >50 MHz clock output frequency
Sub-rate Clock Output (as specified for clock output except for the following)	
Sub-rate Divider Ratios	Full rate divided by 1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 25, 28, 30, 32, 35, 36, 40, 42, 45, 48, 49, 50, 54, 56, 60, 63, 64, 70, 72, 80, 81, 84, 90, 96, 98, 100, 108, 112, 120, 126, 128, 140, 144, 160, 162, 168, 180, 192, 196, 200, 216, 224, 240, 252, 256, 280, 288, 320, 324, 336, 360, 384, 392, 432, 448, 504, 512, 576, 648

Characteristic	Description
Trigger Output (Rear Panel)	
Interface Type	SMA, 50 Ω, DC coupled
Latency	300 ms
Trigger Input (Rear Panel)	
Interface Type	SMA, 50 Ω, DC-coupled to 0 V
Threshold	1.5 V
Minimum Pulse Width	50 ns
Control	
Device Info	Serial number, revision codes available using front-panel display
Control Interface	USB cable (supplied). Unit also provides hub capability giving 3 additional USB ports
Physical and Environmental	
Dimensions (W × H × D)	15.5 in. × 3.75 in. × 13.25 in.
Weight	20 lb.
Temperature	
Operating	0 to 40 °C
Nonoperating	–18 to 60 °C
Relative Humidity	
Operating	20-80% at or below 40 °C
Nonoperating	5-90% at or below 60 °C
Vibration (5-500 Hz)	
Operating	0.2 g RMS
Nonoperating	2.09 g RMS

Specification

The performance of the BERTScope CR Series Option GJ Jitter Spectrum and DCD measurements are listed in the specifications below. The performance of the clock recovery functionality remains identical as listed in the BERTScope CR Series specifications.

Characteristic	Description
Jitter Spectrum	
Minimum Frequency	200 Hz
Maximum Frequency	90 MHz
Minimum Frequency Resolution	200 Hz
Maximum Jitter	Limited only by the ability of the clock recovery to lock with PLL BW at 0.5 MHz and 0.5 dB peaking
Vertical Units	% UI or ps
Vertical Scale	Log or linear
Frequency Scale	Log or linear
Max. Number of Integrated Measurement Frequency Bands	3
Duty Cycle Dependent Jitter	
Units	% UI or ps
Maximum Range	50% UI

Key Specifications

Characteristic	CR125A	CR175A	CR286A	CR175A Option HS	CR286A Option HS
Data Inputs/Outputs					
Input Sensitivity	100 mV single ended (typical) 50 mV differential (typical)			40 mV single ended (typical) 20 mV differential (typical)	
Input Data Rate Coverage	150 Mb/s to 12.5 Gb/s	150 Mb/s to 17.5 Gb/s	150 Mb/s to 28.6 Gb/s	150 Mb/s to 17.5 Gb/s	150 Mb/s to 28.6 Gb/s
Data Insertion Loss	2 dB (min), 2.6 dB (typical), 3 dB (max), up to 12.5 Gb/s*[2]			—	
Data Input Voltage Range	–5 V (min), +5 V (max)			–5 V (min), +5 V (max) 1 V_{p-p} (max)	
Measured Edge Density Accuracy	±1%, up to 14.3 Gb/s, ±3% >14.3 Gb/s				
Equalization Range	0 to 10 dB				
Data Output	Up to 12.5 Gb/s*[2]			—	
Clock and Sub-rate Clock Outputs					
Loop Bandwidth	100 kHz to 12 MHz 200 kHz to 12 MHz above 14.3 GHz – up to 24 MHz with Option XLBW ext. loop BW				
Peaking	0-6 dB, 500 kHz - 12 MHz 0-5 dB, 12 MHz - 24 MHz with Option XLBW				
Intrinsic Jitter (Typical)	250 fs (typ)				
Clock Output Range	Full-rate clock for input data rates to 14.3 Gb/s Half-rate clock for input data rates >14.3 Gb/s				
Sub-rate Divider Ratios	For input data rate to 14.3 Gb/s: Full rate divided by 1, 2, 4, 5, 6, 7, 8, 9, 10, 12, 14, 16, 18, 20, 24, 25, 28, 30, 32, 35, 36, 40, 42, 45, 48, 49, 50, 54, 56, 60, 63, 64, 70, 72, 80, 81, 90, 100, 108, 112, 120, 126, 128, 140, 144, 160, 162, 168, 180, 192, 196, 200, 216, 224, 240, 252, 256, 280, 288, 320, 324, 336, 360, 384, 392, 432, 448, 504, 512, 576, 648 For input data rate >14.3 Gb/s: Full rate divided by 2, 4, 8, 10, 12, 14, 16, 18, 20, 24, 28, 32, 36, 40, 48, 50, 56, 60, 64, 70, 72, 80, 84, 90, 96, 98, 100, 108, 112, 120, 126, 128, 140, 144, 160, 162, 180, 200, 216, 224, 240, 252, 256, 280, 288, 320, 324, 336, 360, 384, 392, 400, 432, 448, 480, 504, 512, 560, 576, 640, 648, 672, 720, 768, 784, 864, 896, 1008, 1024, 1152, 1296				

*[2] Data through path only recommended for use below 12.5 Gb/s. Use external pick-off tees and terminate output connector above 12.5 Gb/s.

Ordering Information

CR125A
12.5 Gb/s Clock Recovery Instrument.

CR175A
17.5 Gb/s Clock Recovery Instrument.

CR286A
28.6 Gb/s Clock Recovery Instrument.

Options

Option	Description	CR125A	CR175A	CR286A
PCIE	PCIe PLL analysis (requires 12GJ, operates at 2.5G and 5G only)	X	X	X
HS	Add High-sensitivity Clock Recovery		X	X
XLBW	Add Extended Loop Bandwidth in the clock recovery	X	X	X
12GJ	Add Jitter Spectrum Analysis from 1.2 to 11.2 Gb/s	X		
17GJ	Add Jitter Spectrum Analysis from 1.2 to 11.2 Gb/s		X	
28GJ	Add Jitter Spectrum Analysis from 1.2 to 11.2 Gb/s			X
CA1	Single Calibration or Functional Verification	X	X	X
C3	Calibration Service 3 Years	X	X	X
R3	Repair Service 3 Years (including warranty)	X	X	X
-R3DW	Repair Service Coverage 3 Years (includes product warranty period); 3-year period starts at time of customer instrument purchase	X	X	X

Accessories

Accessory	Description
CR125ACBL	High-performance Delay-matched Cable Set (required for BERTScope and CRU in SSC applications)
100PSRTFILTER	100 ps Rise Time Filter
BSA12500ISI	Differential ISI Board
PMCABLE1M	Precision Phase-matched Cable Pair, 1 m
SMAPOWERDIV	SMA Power Dividers
BSASATATEE	BSA-SATA-Tee for OOB Signaling
SATATESTSW	Serial ATA Interop Test Suite Automation Software
BSARACK	BSA Rackmount Kits